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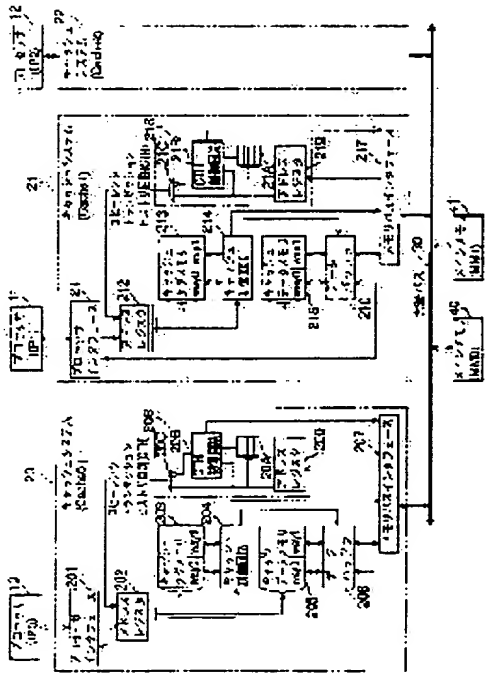
(54) CACHE COHERENCY CONTROL METHOD AND MULTIPROCESSOR SYSTEM USING SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To provide the cache coherency control method which can speedily decide the state of a data block specified by a coherency request issued by another cache system and the multiprocessor system which uses it.
SOLUTION: Cache systems 20, 21, and 22 have similar constitution, and the cache system 20 is equipped with a history table 20A which contains the address of an access request transmitted through a common bus 30 and a history table control circuit 20B. The history table 20B decides whether or not the address of a received access request is put in the table 20A, and inhibits a cache control circuit 204 regarding the access request from operating when the address is stored in the table 20A, but makes the cache control circuit 204 to perform operation regarding the access request when not.



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